User's Guide
SLWU055–May 2008

TSW3070EVM: Amplifier Interface to Current Sink DAC - Arbitrary Waveform Generator Demonstration

The TSW3070 is an evaluation module (EVM) that shows how to use an active interface with the current sink output of the DAC5682Z. The EVM includes the DAC5682Z for digital-to-analog conversion, an OPA695 to demonstrate an active interface implementation using a wide bandwidth operational amplifier and a THS3091/5 to showcase an operational amplifier with large voltage swing. Also included on board are a CDCM7005, VCXO and Reference for clock generation, and linear regulators for voltage regulation. Communication to the EVM is accomplished via a USB interface and GUI software.

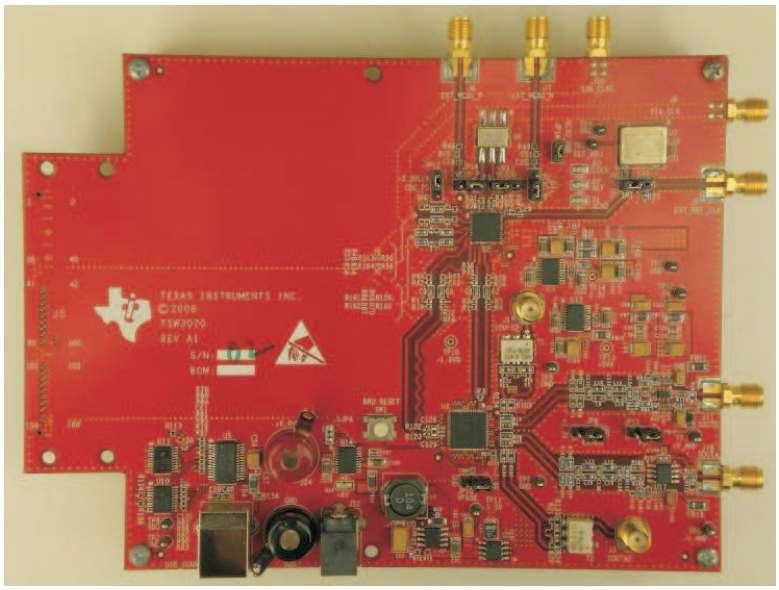

Figure 1. TSW3070EVM

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1 TSW3070EVM Configuration Options

The TSW3070EVM can be configured to evaluate the two active output stages. This section outlines the various component configurations. Based on the configuration, testing and board setup must be altered to accommodate the given components and features.

1.1 DAC Component

The TSW3070EVM uses the 1-GSPS LVDS DAC5682Z with a current sink output.

1.2 Board Configuration

The analog output of the DAC employs a current sink structure which requires the dc common mode of the DAC to be kept at 3.3 V with a maximum compliance voltage at 3.8 V and a minimum voltage at 2.8 V. The resistor bias network between the DAC5682Z and the OPA695 or THS3095 assume that the DAC has maximum current set at 20 mA. For the OPA695 output stage, this network combined with the filter termination provides a combined ac impedance of about 25 Ω, resulting in a maximum voltage of 500 mVpp on each DAC output pin. For the THS3091/5, the network is different and provides a combined 50-Ω load, resulting in a 1-Vpp signal on each of the DAC output pins. By design, in order to preserve the proper dc levels, the DAC coarse gain should be kept at the maximum (15), though deviation by a few steps is generally acceptable with no degradation in performance.

The OPA circuits have been designed to have a combined output gain of 2.2x, whereas the THS3091/5 circuit has a gain of 3.3x. The resistor networks and gain can be modified as necessary for custom applications. However, special care must be taken to ensure that the 3.3-Vdc common mode voltage is maintained at the DAC output and the DAC compliance voltages are met.

1.2.1 Using Optional Passive Transformer Output

The resistor network can be configured such that the DAC output is routed to a transformer which enables measurements of the DAC output to be made using a passive transformer output. Either of the outputs can be configured for this. See Section 9.

1.2.2 Using External Operational Amplifier Supplies

By default, both amplifiers are set up to operate with a ±5 V. This is adequate in most cases for evaluation purposes. However, both the OPA695 and THS3095 can be operated at higher voltages; the OPA can be used with a ±6-V supply, and the THS3095 can be used with a ±15-V supply. Ferrite beads allow the use of a different ±Vamp supply for both amplifiers.

If the THS3095 is being evaluated at voltages higher than ±6 V, the OPA695 power ferrite beads should be removed to isolate the OPA695 from the higher supply voltages. See Section 9.

1.3 VCXO

The CDCM7005 requires a VCXO source to derive its output clock signals. The VCXO is at reference designator U6. There is an onboard 10-MHz reference as well as an onboard 800-MHz VCXO. These can be locked together using the CDCM7005 with the appropriate programming via the DAC5682Z GUI.

An external VCXO clock source can be used. In this mode, the CDCM7005 only acts as a clock divider/buffer to provide the necessary clocks to the TSW3100 LVDS pattern generator, and sampling clock to the DAC5682Z.

2 Block Diagrams

2.1 System Block Diagram

Figure 2 shows the functions on the TSW3070EVM board. The Texas Instruments ICs are listed on the board for reference.

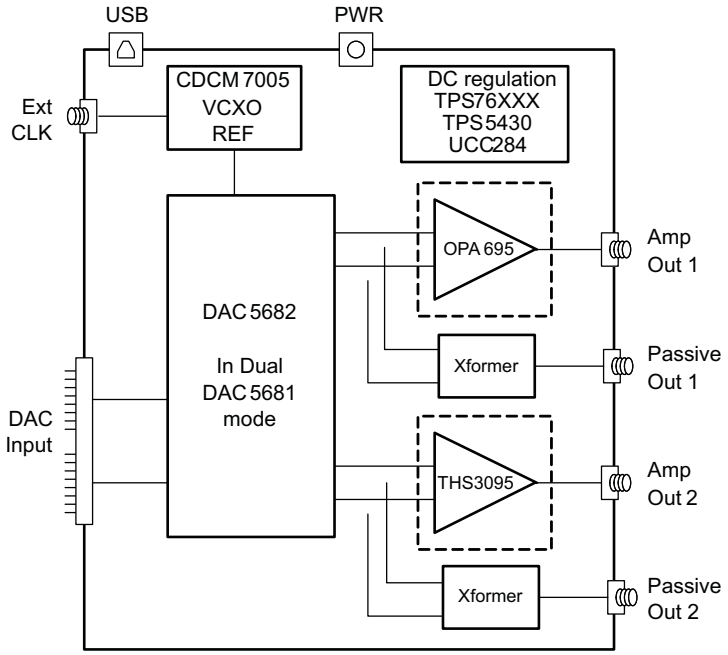


Figure 2. Block Diagram

3 Key Texas Instruments Components

3.1 CDCM7005

The CDCM7005 clock distribution integrated circuit (IC) is used to generate and synchronize the clock outputs to the system. The device has five outputs which can be either LVPECL or LVCMOS and can be divided down by 1, 2, 3, 4, 6, 8, and 16. The divide by 16 can be replaced with a divide by 4 or 8 with a 90 degree phase shift, if desired. This device is used to lock the onboard 800-MHz VCXO and 10-MHz reference. For further information about the CDCM7005 device, see the SCAS793 data sheet.

3.2 DAC5682Z

The DAC5682Z is a 16-bit interpolating dual digital-to-analog converter (DAC) with a high-speed LVDS data interface. The device incorporates a digital complex coarse mixer, independent differential offset control, and I/Q amplitude control. The device can be used with excellent results in baseband mode, low IF mode, and high IF mode. The digital circuits can be manipulated such that it has the functionality of a DAC5681. For further information about the DAC5682Z device, see the SLLS853 data sheet.

3.3 TPS76xxx, TPS5430, UCC284-5

The TPS76xxx devices provide 1.8-V, 3.3-V, and 5-V linear regulation for the DAC5682Z, CDCM7005, and V+ amplifier supplies. The TPS5430 generate –5.5 V from 6-V input followed by the UCC284-5 which provides linear -5-V regulation for the V– amplifier supply. More information about the TPS5430 and UCC284-5 devices can be found in SLVS632 and SLUS234 data sheets, respectively.

3.4 OPA695 and THS3091/5

These both provide the differential-to-single-ended conversion for the DAC5682Z output. The OPA695 is a wide bandwidth (1400 MHz) high-performance operational amplifier (see data sheet SBOS693). The THS3095 is high-performance operational amplifier capable of driving large voltages (20+ Volts). Data sheet SLOS423 provides more information about the THS3091/5 device.

Both DAC outputs have optional transformer outputs to bypass the operational amplifiers, if needed. There are also options to bypass the onboard supplies to use higher external operational amplifier supplies.

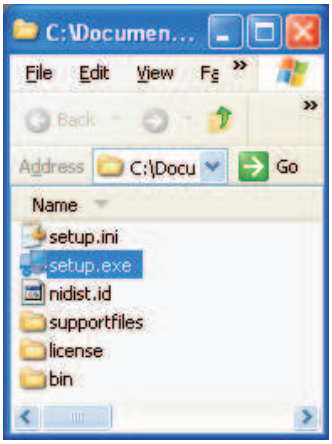
The amplifier circuits can be further optimized by following the guidelines in the application report SBAA135. This optimization can be performed once the final filter and gain components have been selected.

4 Software Installation

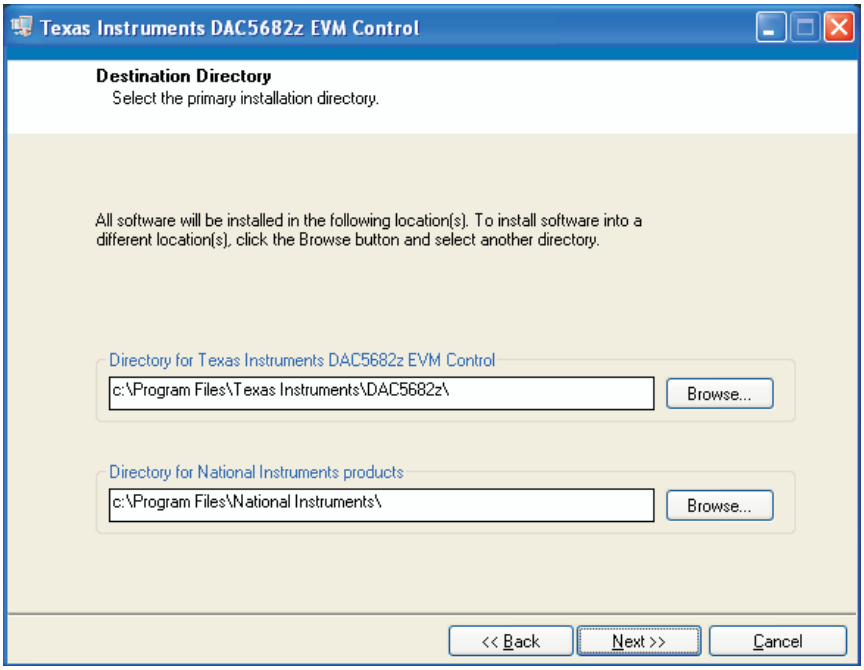
The enclosed CD-ROM contains all of the necessary software that is needed for the host personal computer (PC) to control the DAC5682Z and CDCM7005 on the TSW3070EVM. The interface software is a graphical user interface (GUI) that allows all the registers to be programmed in the CDCM7005 and the DAC5682Z. Once the software is installed, the GUI is accessible from the Start → All Programs → Texas Instruments DACs → DAC5682z EVM Control. This GUI was originally used for the TSW3082 (DAC5682+RF modulator) but is also applicable for the TSW3070EVM.

4.1 DAC5682Z USB Control Software Installation

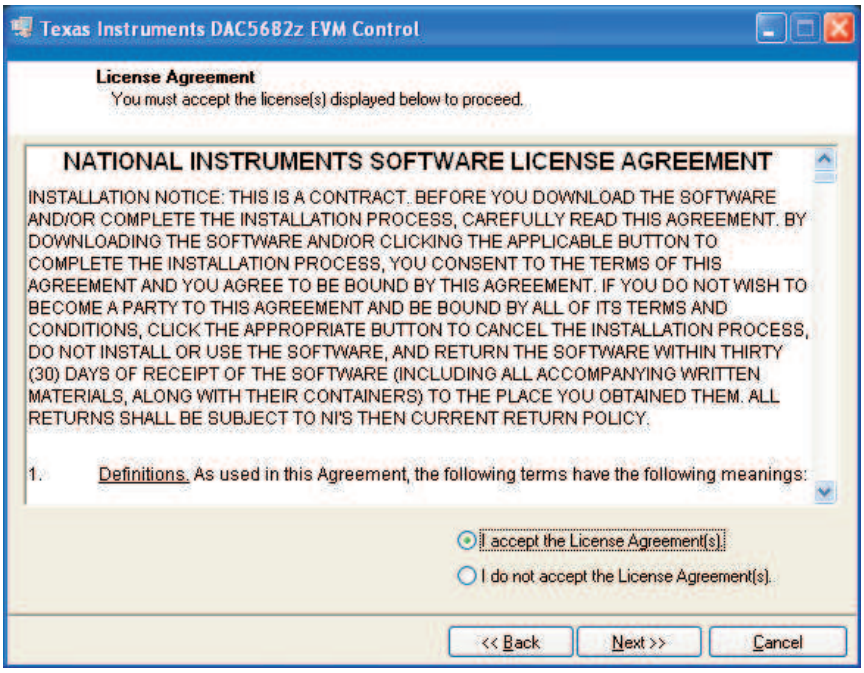
Copy the DAC5682z software from the provide CD to a local drive on a PC. Execute the **setup.exe** file. This starts the DAC5682Z control software installation.



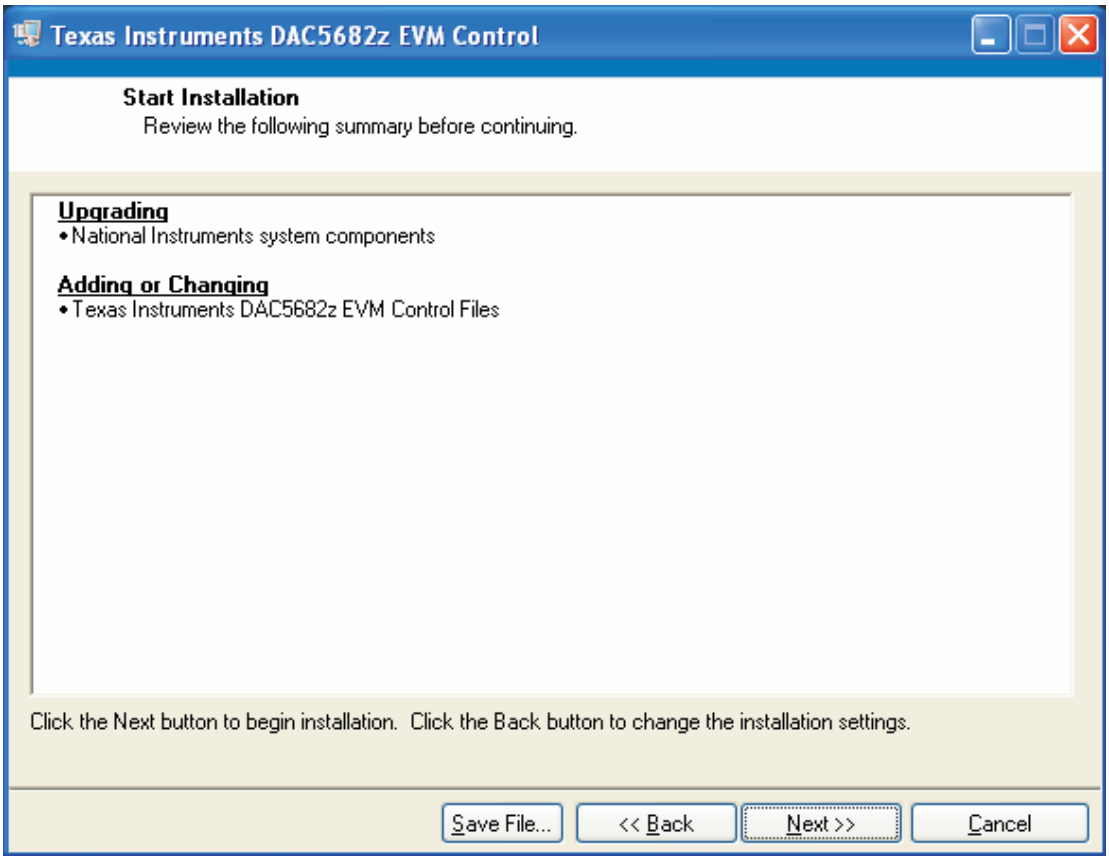
The destination directory for the installer is displayed. It is recommended to leave the default folder location. Any necessary folders are created by the installation if they do not exist. Click **Next**



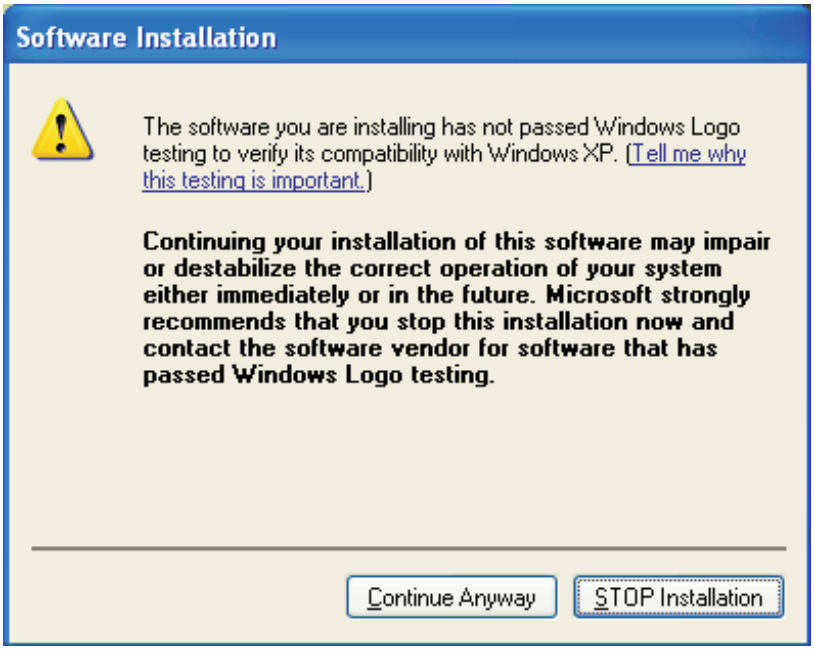
Accept the EULA, and click **Next**



Click **Next** again to start the installation



Click **Continue** to complete the installation.

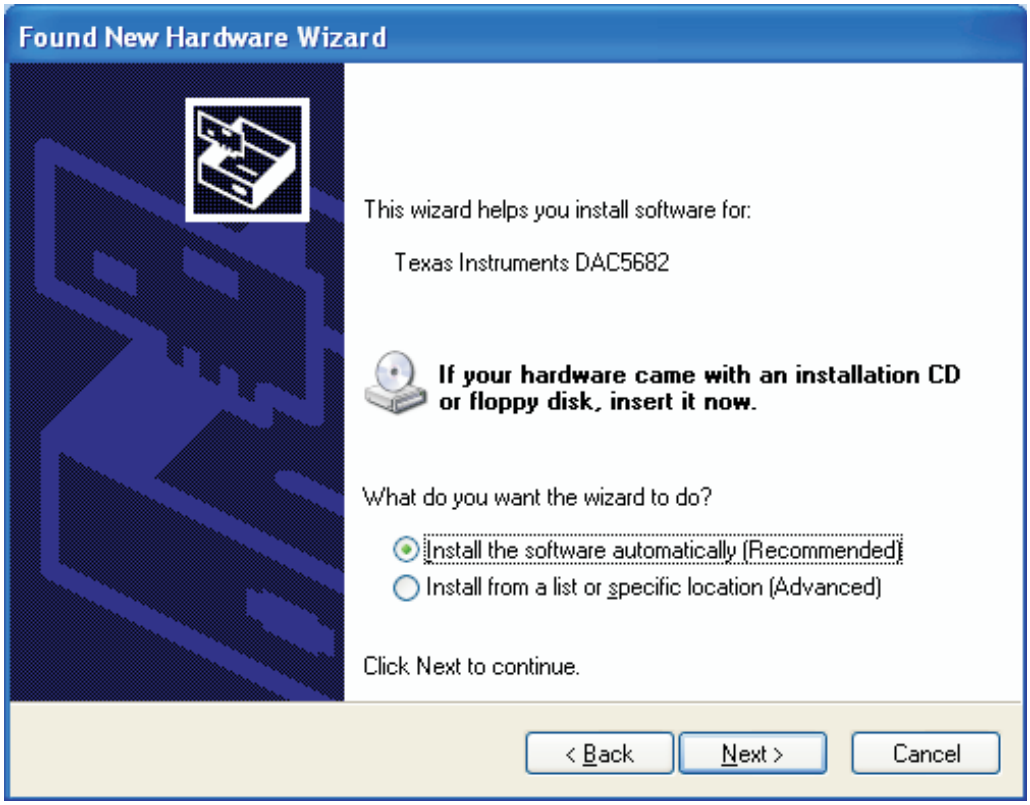


Restart the PC as directed.

4.2 DAC5682Z EVM Driver Installation

Once the PC has restarted, connect the provided USB cable to the PC and connector J13 of the evm. Power up TSW3070EVM using the provide +6V power supply. After power is applied, the USB driver installation process will start. The hardware wizard detects the evm. When asked if it should connect to the update server to locate drivers, click **NO**, and then **Next**

Install the drivers Automatically as recommended. Click **Next.**



Click Continue for the digital signature. The drivers were installed during the software installation and will be installed automatically. If asked to overwrite newer drivers, click **Yes**. Click **Finish** to complete the driver installation. If a DAC5682 evm driver has been previously installed, Windows Hardware Wizard may not require the drivers to be installed and these steps will not be required.

The software can now be started from Start → All Programs → Texas Instruments DACs → DAC5682z EVM Control.

5 Software Introduction

The DAC5682Z EVM control software allows you to:

- Configure the DAC5682Z and CDCM7005 registers
- Save and load these register settings to/from the text files
- Visualize the data path through the DAC5682Z
- Download a pattern to the Texas Instruments TSW3100 Pattern Generator System – an FPGA-based LVDS/CMOS pattern generator (link to TSW3100 EVM folder)

5.1 Modes of Operation

The software has five main settings that allow you to modify the functionality of the active panels. You can switch between these settings by selecting one of the options on the Menu box. The five settings are described in Table 1.

Table 1. Software Main Settings

Setting	Top Panel	Bottom Panel
EVM Home	EVM and DAC5682Z serial information. EVM communication status	Not used
DAC5682Z Diagram	DAC5682Z register settings	DAC5682Z data path under the current register settings

Table 1. Software Main Settings (continued)

Setting	Top Panel	Bottom Panel
Register Config	DAC5682Z register settings	CDCM7005 register settings
TSW3100 Config	DAC5682Z register settings	TSW3100 settings
Help	DAC5682Z register settings	DAC5682Z data path and help window

5.2 Software Boxes

The DAC5682Z software interface controls are divided into boxes. The functionality of these boxes is described in Table 2.

Table 2. Software Box Descriptions

Box	Description
Menu	Switch between main functionality settings.
Home	Show serial information and EVM status.
USB/Readback	Reset the USB port to begin a new data session. Disable DAC5682Z read capabilities (simulation mode).
DAC5682Z Register Table	Show the DAC5682Z register settings in binary and hex formats.
DAC5682Z Register Configuration	Read/Write DAC5682Z register configuration.
CDCM7005 Register Configuration	Write CDCM7005 register configuration (no read capability).
DAC5682Z Diagram	Graphical representation of the DAC5682Z data path under current register configuration.
TSW3100 Configuration	Control a TSW3100 pattern generation system – refer to TSW3100 users guide for more information
Help	Display information on the DAC5682Z register configuration box controls.

A diagram of each of these Menu choices is shown in the following illustrations.

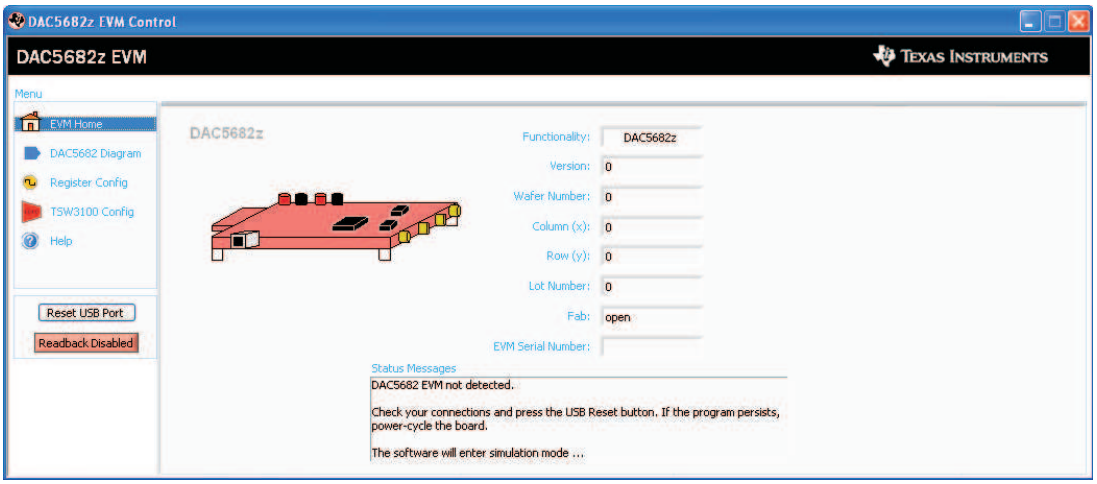


Figure 3. Home Menu Showing EVM Status

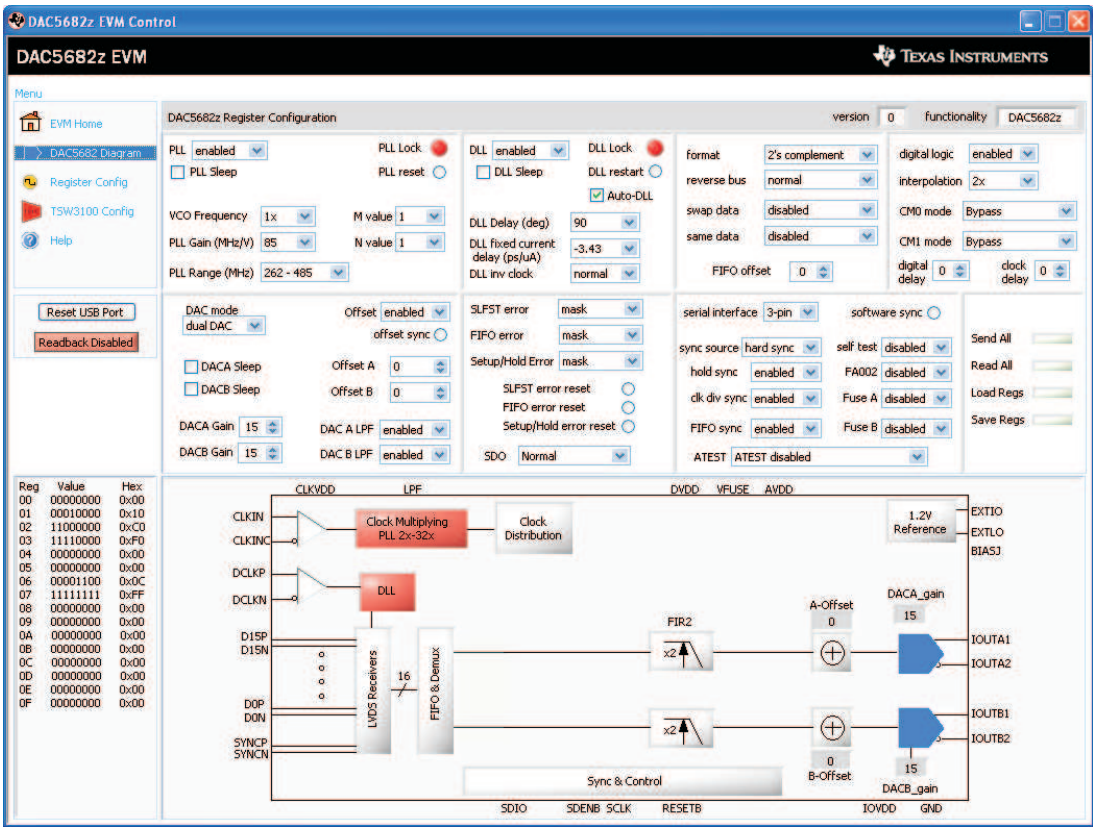


Figure 4. DAC5682Z Register Configuration and Block Diagram Menu

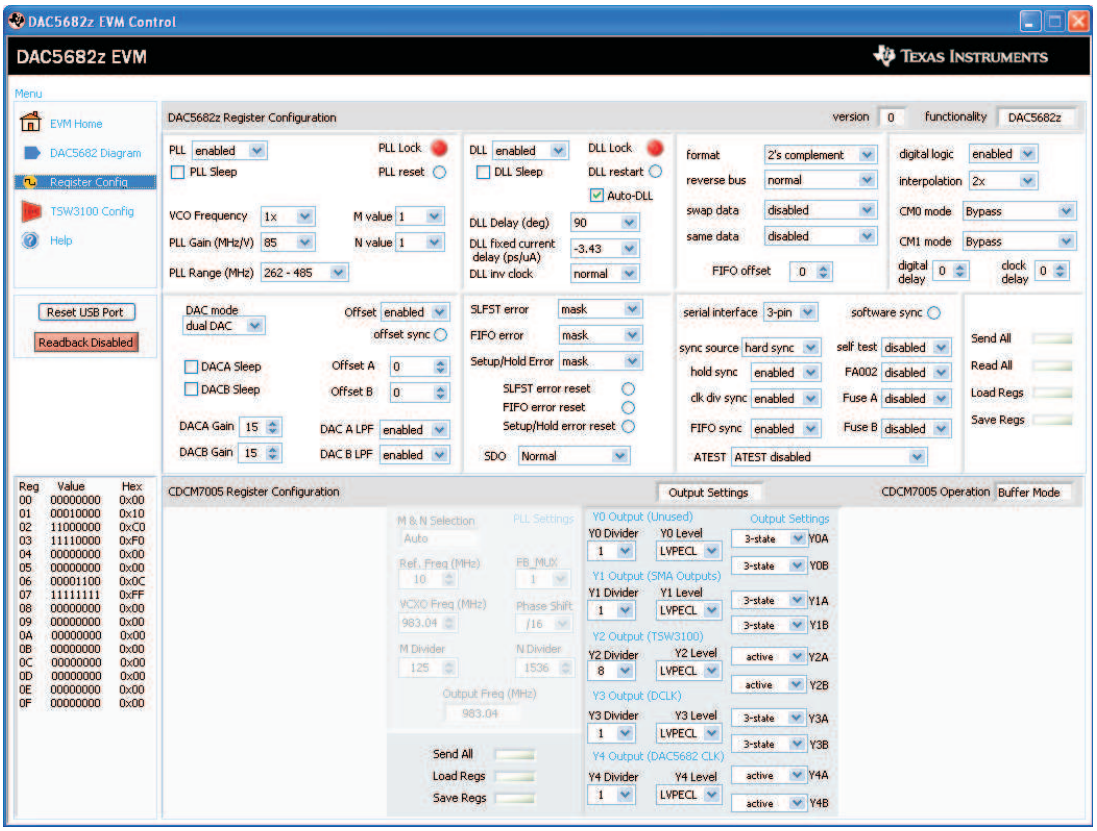


Figure 5. DAC5682Z Register and CDCM7005 Configuration Menu

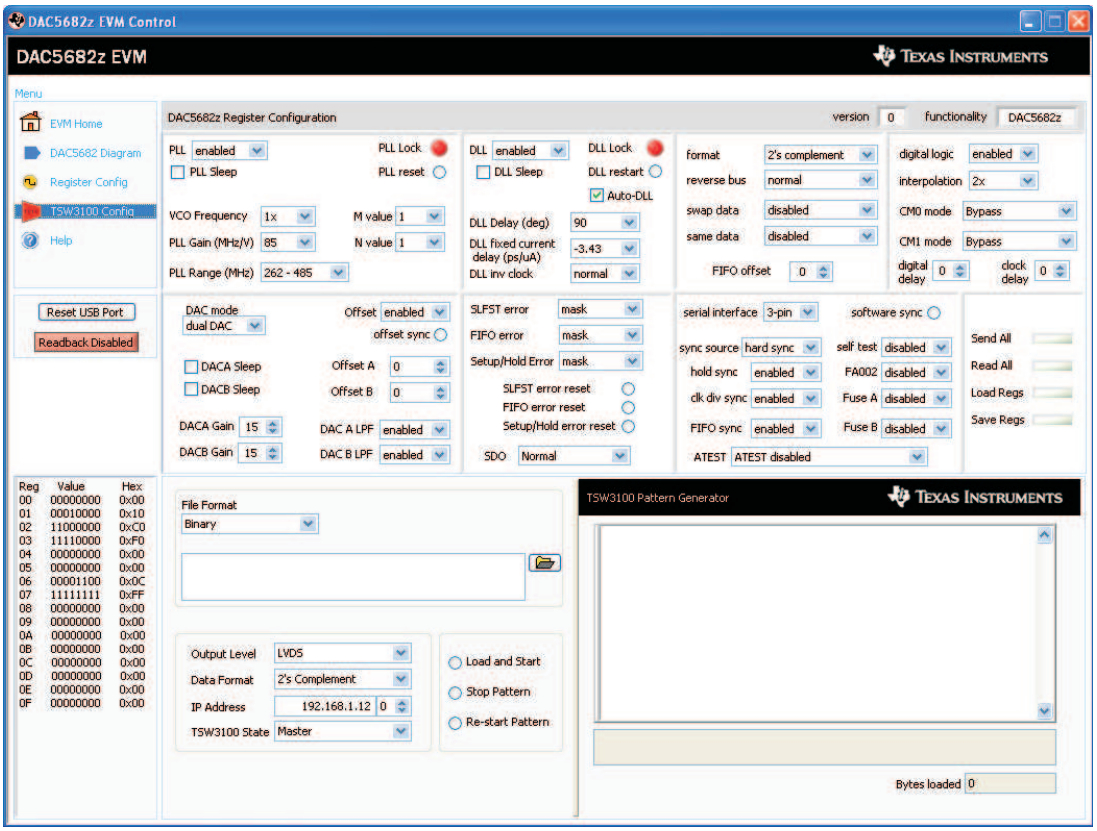


Figure 6. DAC5682Z Register Configuration and TSW3100 Pattern Generator Control Menu.

The TSW3100 can be loaded with a custom pattern file using the GUI options. For further details on the format of this file, see the TSW3100 user's guide.

5.3 Complete Software Overview

Table 3 contains a complete reference of all the software controls.

Table 3. Software Feature Descriptions

Control Name	Input/Output	Description
MENU BOX		
EVM Home	Input	Displays EVM Home Box.
DAC5682Z Diagram	Input	Displays DAC5682Z Register Configuration and DAC5682Z Diagram boxes.
Register Config	Input	Displays DAC5682Z and CDCM7005 Register Configuration boxes.
TSW3100 Config	Input	Displays DAC5682Z Register Configuration and TSW3100 Configuration boxes.
Help	Input	Displays Help box.
HOME BOX		
Functionality	Output	DAC device.
Version	Output	Chip version.
Wafer number	Output	DAC5682Z wafer number.
Column (x)	Output	DAC5682Z column position.
Row (y)	Output	DAC5682Z row position.
Lot Number	Output	DAC5682Z lot number.
Fab	Output	Fab where the DAC5682Z was manufactured.

Table 3. Software Feature Descriptions (continued)

Control Name	Input/Output	Description
EVM Serial Number	Output	Serial number of the EVM.
Status Messages	Output	Displays the status of the communication session.
USB/READBACK BOX		
Reset USB Port	Input	Begins a new USB session. Press this if you see a status error message.
Readback	Input/Output	Disables DAC5682Z register reads (simulation mode)
DAC5682Z REGISTER TABLE BOX		
Register Table	Output	Displays the DAC5682Z register configuration.
DAC5682Z REGISTER CONFIGURATION BOX		
PLL SETTINGS		
PLL	Input/Output	When disabled, the PLL is bypassed
PLL Sleep	Input/Output	When set, the PLL is put into sleep mode.
PLL Lock	Output	Turns green when the internal PLL is locked.
PLL Reset	Input/Output	When set, the PLL loop filter is pulled down to 0V. Toggle to restart the PLL if an over-speed lock-up occurs.
VCO Frequency	Input/Output	When set to 2x, the PLL clock output is 1/2 the PLL VCO frequency. Used to run the VCO at 2X the needed clock frequency to reduce phase noise for lower input clock rates.
PLL Gain (MHz/V)	Input/Output	Used to adjust the PLL Voltage Controlled Oscillator (VCO) gain.
PLL Range (MHz)	Input/Output	Sets the PLL VCO frequency range.
M value	Input/Output	M portion of the M/N divider of the PLL.
N value	Input/Output	N portion of the M/N divider of the PLL. This value should be chosen to divide down the input CLKIN to maintain a maximum PFD of 160 MHz.
DLL SETTINGS		
DLL	Input/Output	When disabled, the DLL is bypassed and the LVDS data source is responsible for providing correct setup and hold timing.
DLL Sleep	Input/Output	When set, the DLL is put into sleep mode.
Auto-DLL	Input	When set, the DLL is restarted automatically when there is a change in the DLL settings, so there is no need to press the DLL restart control.
DLL Lock	Output	Turns green when the internal DLL is locked.
DLL restart	Input/Output	Restarts the DLL
DLL Delay (deg.)	Input/Output	Used to manually adjust the DLL delay = from the DLL fixed current delay.
DLL fixed current delay (ps/µA)	Input/Output	Adjusts the DLL delay line bias current. Used in conjunction with the DLL inv clock to select appropriate delay range for a given DCLK frequency
DLL inv clock	Input/Output	Used to invert the internal DLL clock to force convergence to a different solution. This can be used in the case where the DLL delay adjustment has exceeded the limits of its range
INPUT SETTINGS		
format	Input/Output	Selects between 2's complement and offset binary formats.
reverse bus	Input/Output	When enabled, reverses the LVDS input data bus so that the MSB to LSB order is swapped.
swap data	Input/Output	When enabled, the A/B data paths are swapped prior to routing to the DACA and DACB outputs.
same data	Input/Output	When enabled, the data routed to DACA is also routed to DACB.
FIFO offset	Input/Output	Sets the FIFO's output pointer location, allowing the input pointer to be shifted –4 to +3 positions upon SYNC. Default offset is 0 and is updated upon each sync event.
DIGITAL SETTINGS		
digital logic	Input/Output	Enables the interpolation filters on the device.
interpolation	Input/Output	Selects the interpolation rate.
CM0 mode	Input/Output	Determines the mode of FIR0 and CMIX0 blocks. Since CMIX0 is located between FIR0 and FIR1, its output is half-rate. Settings apply to both A and B channels.

Table 3. Software Feature Descriptions (continued)

Control Name	Input/Output	Description
CM1 mode	Input/Output	Determines the mode of FIR1 and final CMIX1 blocks. Settings apply to both A and B channels.
digital delay	Input/Output	DAC data delay adjustment (0–3 periods of the DAC clock). This can be used to adjust system level output timing. The same delay is applied to both DACA and DACB data paths.
clock delay	Input/Output	Changes the number of buffers that the input clock goes through. This allows some adjustment of the setup/hold of the handoff between the receivers and the digital section.
— DAC SETTINGS		
DAC mode	Input/Output	Selects between dual DAC mode and single DAC mode. It is also used to select input interleaved data (dual DAC mode).
DACA Sleep	Input/Output	When set, DACA is put into sleep mode.
DACB Sleep	Input/Output	When set, DACB is put into sleep mode. DACB is not automatically set into sleep mode when configured for single DAC mode. Set this control in single DAC mode to get the lowest power configuration since the output is on DACA only.
DACA Gain	Input/Output	Scales the DACA output current in 16 equal steps.
DACB Gain	Input/Output	Scales the DACB output current in 16 equal steps.
Offset	Input/Output	When enabled, the Offset A and Offset B values are summed into the DACA and DACB data paths. This provides a system-level offset adjustment capability that is independent of the input data.
offset sync	Input/Output	Transfers the Offset A and Offset B values to the registers used in the DACA and DACB offset calculations. This control is enabled automatically every time there is a change in the Offset A or Offset B values.
Offset A	Input/Output	Offset adjustment value for the A data path.
Offset B	Input/Output	Offset adjustment value for the B data path.
DAC A LPF	Input/Output	Enables a 95-kHz low-pass filter corner on the DACA current source bias. When disabled a 472-Hz filter corner is used.
DAC B LPF	Input/Output	Enables a 95-kHz low-pass filter corner on the DACB current source bias. When disabled a 472-Hz filter corner is used.
— ERROR SETTINGS		
SLFST Error	Input/Output	Masks out SLFTST Errors
FIFO Error	Input/Output	Masks out FIFO Errors
Setup/Hold Error	Input/Output	Masks out Setup/Hold Errors.
SLFST error reset	Input/Output	Asserted when the Digital Self Test (SLFTST) fails. Clear to reset a SLFST error.
FIFO error reset	Input/Output	Asserted when the FIFO pointers overrun each other causing a sample to be missed. Clear to reset a FIFO error.
Setup/Hold error reset	Input/Output	Any received data pattern other than 0xAAAA or 0x5555 causes this bit to be set. Clear to reset a Setup/Hold error.
SDO	Input/Output	Selects the output signal on the SDO pin.
—SYNC SETTINGS		
Serial interface	Input/Output	Selects between 3 pin or 4 pin serial interface mode.
sync source	Input/Output	Selects the synchronization signal source. If soft sync is selected the software sync control is used as the only synchronization input and the LVDS external SYNC input pins are ignored.
software sync	Input/Output	This control can be used as a substitute for the LVDS external SYNC input pins for both synchronization and transmit enable control.
hold sync	Input/Output	Enables the sync to the FIFO output HOLD block.
clk div sync	Input/Output	Enables the clock divider sync.
FIFO sync	Input/Output	Enables the FIFO offset sync.
self test	Input/Output	Enables a Digital Self Test (SLFTST) of the core logic
FA002	Input/Output	Keep disabled. Used only for factory test purposes.
Fuse A	Input/Output	Keep disabled. Used only for factory test purposes.
Fuse B	Input/Output	Keep disabled. Used only for factory test purposes.

Table 3. Software Feature Descriptions (continued)

Control Name	Input/Output	Description
ATEST	Input/Output	Keep disabled. Used only for factory test purposes.
– SEND/SAVE SETTINGS		
Send All	Input	Writes all registers to the DAC5682Z device.
Read All	Input	Reads all registers from the DAC5682Z device. It is rarely necessary to use this as the registers are read every time a DAC5682Z control changes.
Load Regs	Input	Loads a DAC5682Z register configuration from a text file. Files need to consist of a single column with the register values in hexadecimal format.
Save Regs	Input	Saves a DAC5682Z register configuration to a text file.
CDCM7005 REGISTER CONFIGURATION BOX		
—GENERAL SETTINGS		
Output Settings	Input	Switches the display between the CDCM7005 output register settings and advanced register settings.
CDCM7005 Operation	Input	Select “Buffer Mode” when there is no VCXO installed or the VCXO is enabled. In this case the CDCM7005 operates as a buffer. Select “PLL Mode” when a VCXO is being used by the CDCM7005.
— PLL SETTINGS		
M & N Selection	Input	When Auto is selected the M and N divider values are calculated automatically based on the Reference and VCXO frequencies.
Ref. Freq. (MHz)	Input	Frequency of the reference oscillator given to the CDCM7005.
VCXO Freq. (MHz)	Input	Frequency of the VCXO used.
M Divider	Input/Output	M divider value.
N Divider	Input/Output	N divider value.
FB_MUX	Input/Output	Feedback MUX select.
Phase Shift	Input	Phase shift select.
Output Freq (MHz)	Output	Output frequency of the CDCM7005 based on the Reference and VCXO frequencies, and M and N values. If this frequency differs from the VCXO frequency it is displayed in red.
— OUTPUT SETTINGS		
Y0-Y4 Dividers	Input	Selects the output dividers of the CDCM7005 outputs.
Y0-Y4 Levels	Input	Selects between CMOS or LVPECL levels of the CDCM7005 outputs.
Y0-Y4 States	Input	Selects the operating state of the CDCM7005 outputs.
— ADVANCED SETTINGS		
Advanced Registers	Input	CDCM7005 advanced registers. See the CDCM7005 datasheet for more information on these registers
TSW3100 CONFIGURATION BOX		
File Format	Input	Selects between binary and 16-bit signed integer format. If binary is selected the file must comply with the requirements described on the TSW3100 documentation. If integer format is selected, the file must consist of a single column for a real signal or two columns for a two-channel or complex signal.
Column Delimiter	Input	Indicates the column separator used in the two-channel or complex integer input file.
File Browser	Input	Used to browse the input pattern file.
Output Level	Input	Selects between LVDS or CMOS outputs. Only LVDS is available for the DAC5682Z
Data Format	Input	Selects between 2s complement or offset binary format.
IP Address	Input	IP address of the TSW3100 pattern generator.
TSW3100 State	Input	Selects between Master or Slave mode. The default state is Master mode. See the TSW3100 documentation for more information.
Load and Start	Input	Select this to load a pattern file and start the TSW3100.
Stop Pattern	Input	Select this to stop the pattern.
Re-start Pattern	Input	Select this to re-start the pattern. A loaded must be loaded in memory for this to work.
Command	Output	Shows a list of the commands sent to the TSW3100.

Table 3. Software Feature Descriptions (continued)

Control Name	Input/Output	Description
Status	Output	Status of the TSW3100 transaction.
Bytes loaded	Output	Displays the number of bytes loaded to the TSW3100.

6 TSW3070EVM Introduction

The TSW3070EVM was designed to provide a robust yet flexible evaluation system for the DAC5682Z as used in an arbitrary waveform generation system. The EVM includes, in addition to the DAC5682Z, a CDCM7005 for clock distribution, an OPA695, and THS3091/5 active output interface designed to drive into a 50-Ω termination. For a complete hardware description, consult the schematics and layout documents included on the provided CD.

6.1 Jumper Settings

The TSW3070EVM has onboard jumpers that allow you to modify the board configuration. Table 4 explains the functionality of the jumpers.

Table 4. Jumper List

Jumper	Label	Function	Condition	Default
JP8	EXTLO	Internal (GND) or external (3.3V) voltage reference	GND	Pin 2-3
JP10	VFUSE	Factory use only. Connect to 1.8VDD for normal operation.	1.8 VDD	Pin 1-2
JP11	THS PD	Low-active power down of THS3091/5	+Vamp	Pin 1-2
JP12	CDC_PD	Low-active power down of CDCM7005	3.3 VCLK	Pin 1-2
JP13	VCXOB	Choose internal VCXO or external VCXO INB	Internal VCXO	Pin 1-2
JP14	VCXO_P	Choose internal VCXO or external VCXO positive input	Internal VCXO	Pin 1-2
JP15	VCXO_N	Choose CDCM7005 or external VBB	CDCM7005	Pin 1-2
JP16	REF_CLK	Choose internal 10-MHz ref or external ref	Internal Ref	Pin 2-3
JP19	+3.3VCLK	VCXO power supply	VCXO on	Pin 1-2

6.2 Input/Output Connectors

Table 5 lists the input and output connectors.

Table 5. Input and Output Connections

Reference Designator	Label	Connector Type	Description
J1	IOUTB2	SMA	DACB transformer output. Optional IOUTB2 output.
J3	IOUTA2	SMA	DACA transformer output. Optional IOUTA2 output.
J5		SAMTEC	Input LVDS data to DAC682z. Output clock to data source.
J6	EXT_VCXO_P	SMA	External main clock input.
J7	EXT_VCXO_N	SMA	External VCXO negative connection. Not required.
J8	Y2A_CLK	SMA	Optional CDCM7005 clock output.
J9	EXT_REF_C	SMA	External reference clock input.
J10	Y2B_CLK	SMA	Optional CDCM7005 clock output.
J13	USB_CONN	USB	USB connector for software communication.
J12/J25	6V input & Return	Banana Plug	6V input voltage pair
J16	THS3091/5 OUT	SMA	Output of the THS3091/5 amplifier
J11	OPA695 OUT	SMA	Output of the OPA695 amplifier

6.3 USB Interface

The TSW3070EVM contains a 4-pin USB port connector to interface to a USB 1.1 or later compliant USB port. Programming of the CDCM7005 and DAC5682Z is accomplished through this port.

6.4 Power Management

The TSW3070EVM requires an input of 6 VDC either from the banana connectors or the supplied 6-V wall supply. A current rating of at least 2 A is recommended for the 6-V supply. The rest of the supplies: 3.3, 1.8, ±5V are all generated on the board with linear regulators.

7 Demonstration Kit Test Configuration Test Equipment

7.1 Test Setup

The test setup for the TSW3070EVM is shown in Figure 7. This setup shows the TSW3100 pattern generator supplying an LVDS signal to the TSW3070EVM. (see the TSW3100 product folder).

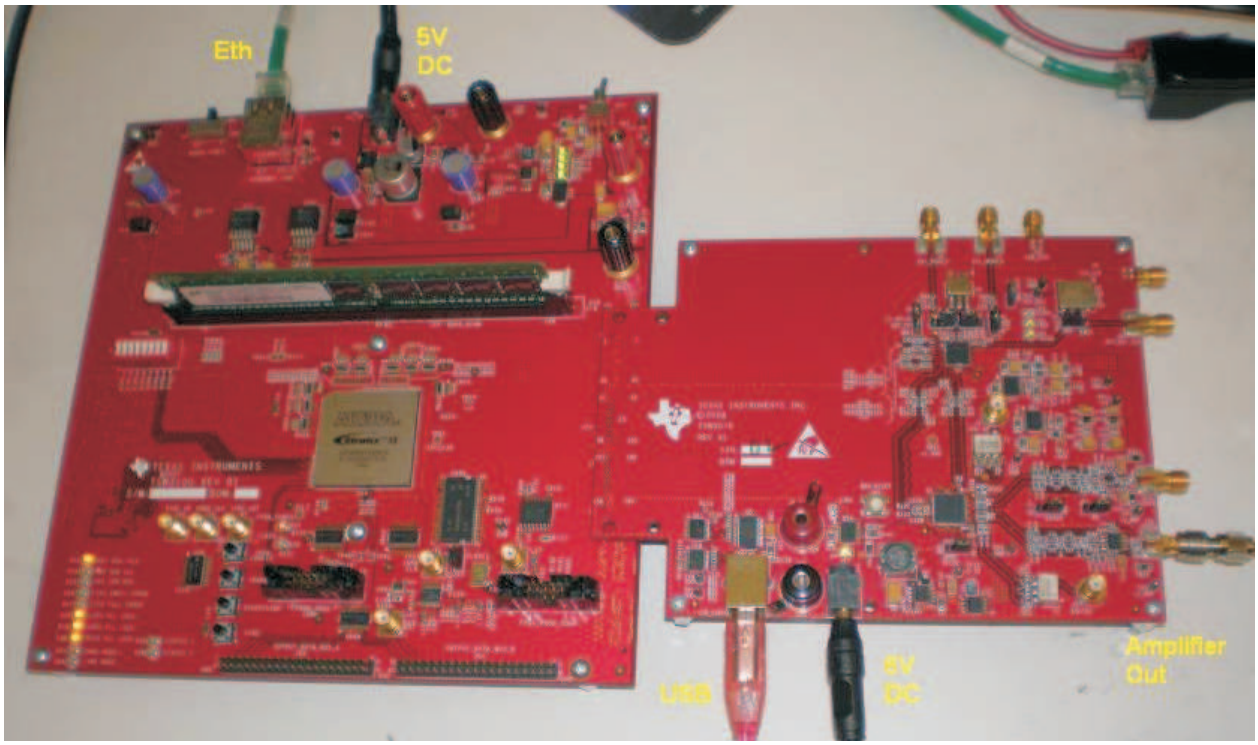


Figure 7. TSW3070EVM Driven by TSW3100 Pattern Generator

7.2 Test Equipment

The following test equipment is required for testing the .TSW3070EVM. Some other equipment may be used; however, results may vary due to limitations of the instruments.

- Power supply 6 VDC @ 2 A.
- Spectrum Analyzer: Rhode & Schwarz FSU, FSQ, or equivalent.
- Pattern generator: TSW3100 using LVDS mode, or some other LVDS capable pattern generator.
- Oscilloscope: Probe clock and data lines for trouble shooting, measure voltage waveform in time domain.
- Digital voltmeter to verify signal levels.

7.3 Calibration

In order to measure the proper output power, the insertion loss of the analyzer cable must be calibrated. Measure a calibrated 0-dBm source to see how much loss is in the cable at the frequency of interest.

7.4 Typical Performance Measurements

The TSW3070EVM ac measurements at the transformer outputs can be used to verify the performance of the DAC5682Z if necessary, or if a reference signal is needed when measuring the performance at the OPA695 or THS3091/5 output. The OPA695 and THS3091/5 are both implemented in a differential-in to single-ended-out configuration. The gain of the OPA695 has been set to 2.2x, and the THS3091/5 has been set to a gain of 3.3x. The input on the OPA695 has an effective 25-Ω load on a 20-mA ac signal. The input of the THS3091/5 has an effective 50-Ω load with a 20-mA ac signal.

Using the TSW3100 in the Multi-Tone GUI mode, a single tone can be generated and measured at both outputs. This measurement must be verified first before any other testing or modification of the board is attempted to ensure that all hardware and software interfaces are operational. The OPA695 output is about 1.8 Vpp, whereas the THS3095 is about 5 Vpp.

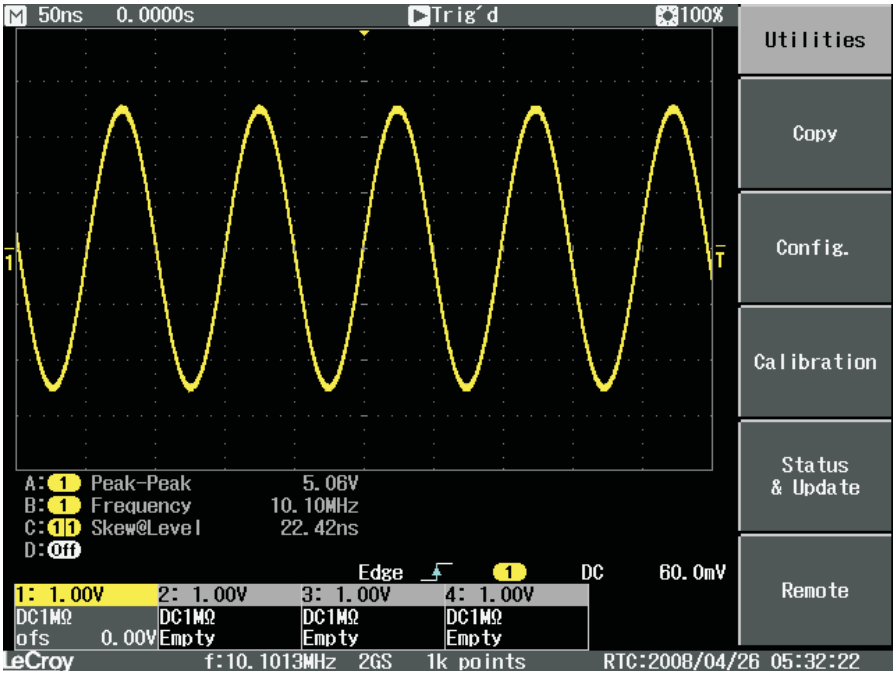


Figure 8. Typical THS3091/5 Voltage Output, Default Gain 3.3x

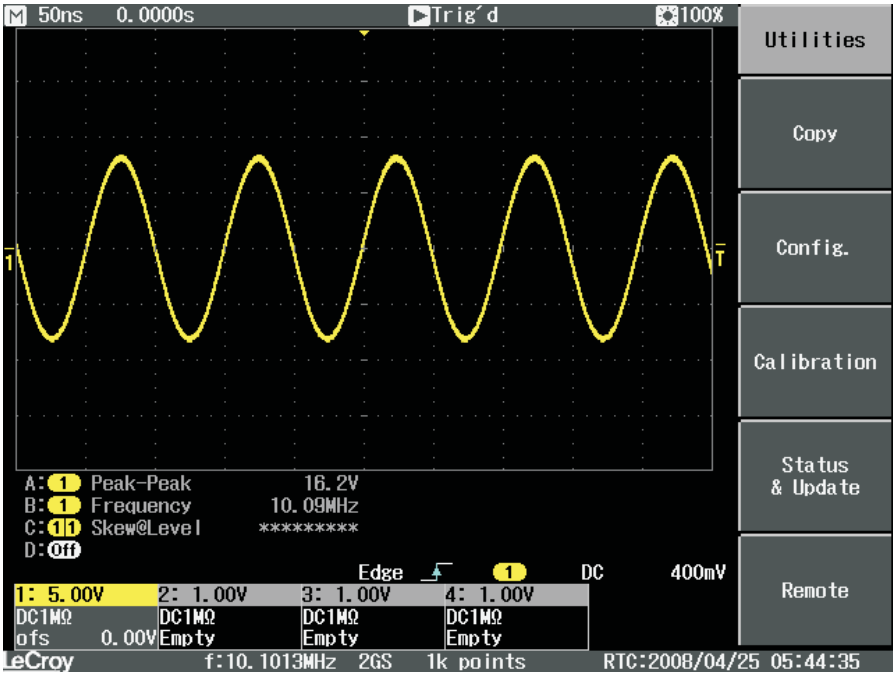


Figure 9. THS3091/5 With +/-15-V External Supplies, 50-Ω Input, Gain at 10x

A low-pass filter (LPF) is between the DAC outputs and the OPA695 and THS3091/5. This prevents any higher frequency DAC images from affecting performance of the amplifiers. The wide bandwidth OPA695 is typically operated at lower gains with smaller output swings with a wider input LPF, about 200 MHz. The THS3095 is normally operated at larger gains (larger feedback resistor) and larger output swings which results in narrower output bandwidth. Consequently, the LPF for the THS3091/5 is set lower at 100 MHz. Both LPFs are 50-Ω differential, fifth-order Chebyshev filters with a 0.1-dB ripple. Filter design can be done according to application report SLWA053 with freely available tools.

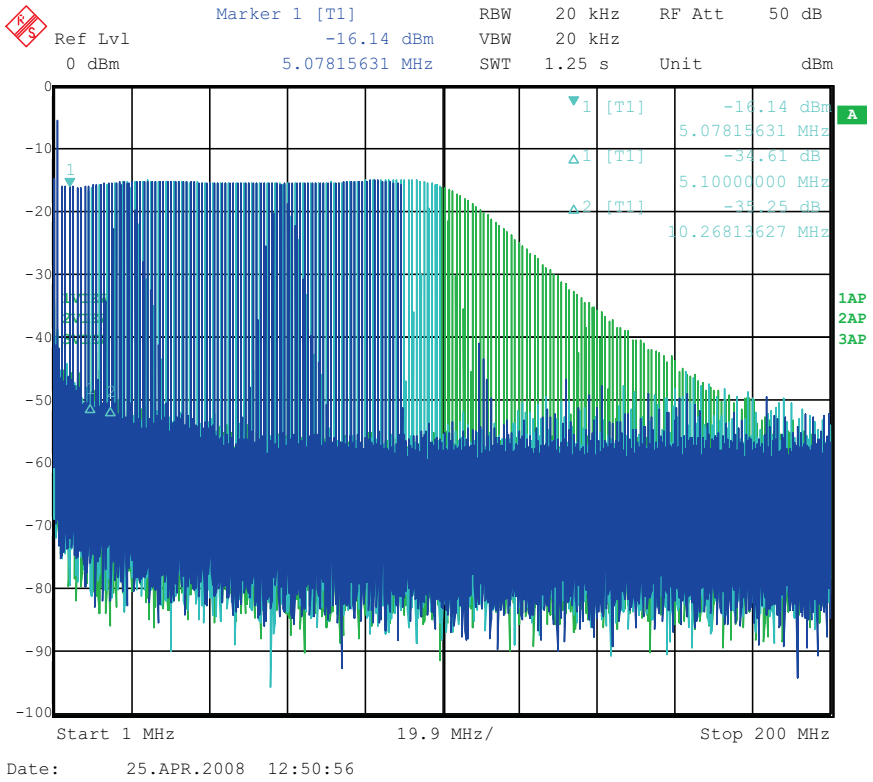


Figure 10. THS3091/5 LPF Filter Shape Evaluated With Multi-tone Input Signal From the TSW3100 Pattern Generator

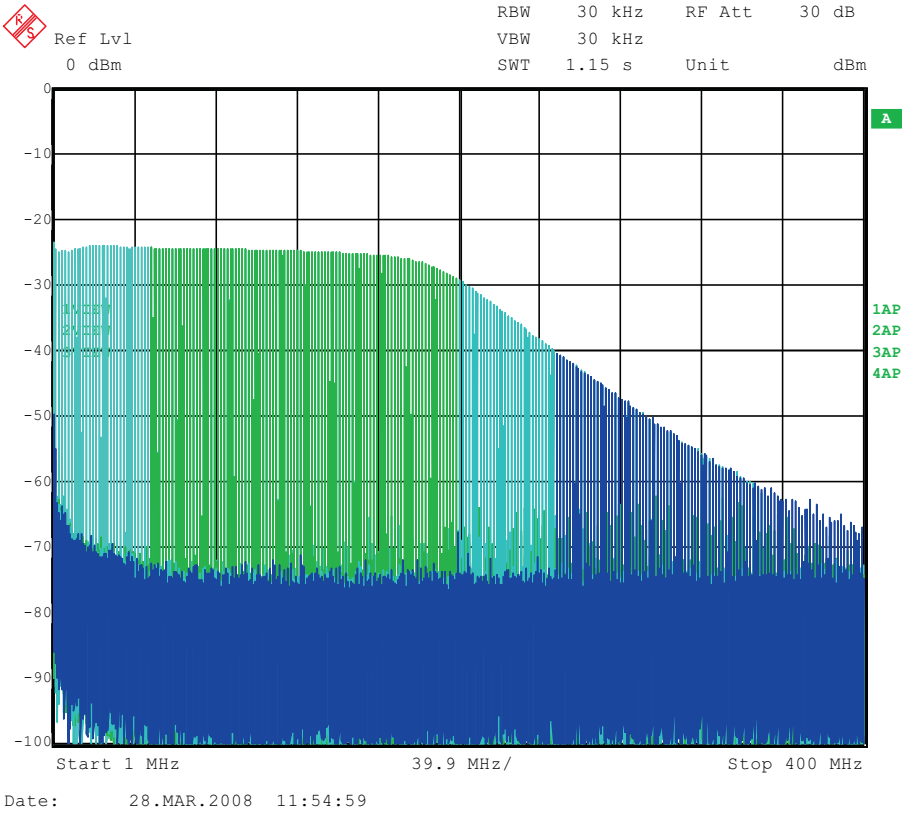


Figure 11. OPA695 LPF Filter Shape Evaluated With Multi-tone Signal

Some typical IMD3 data was obtained for both devices configured with 25-Ω input impedances and identical gains of 2.2x using ±5-V onboard supplies.

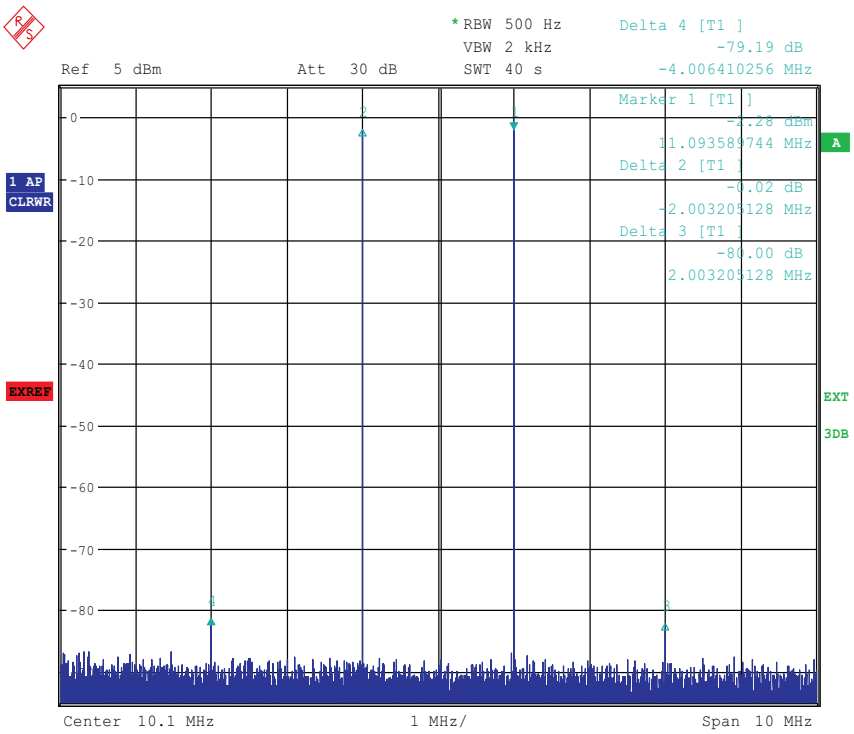


Figure 12. IMD3 Plot for THS3095

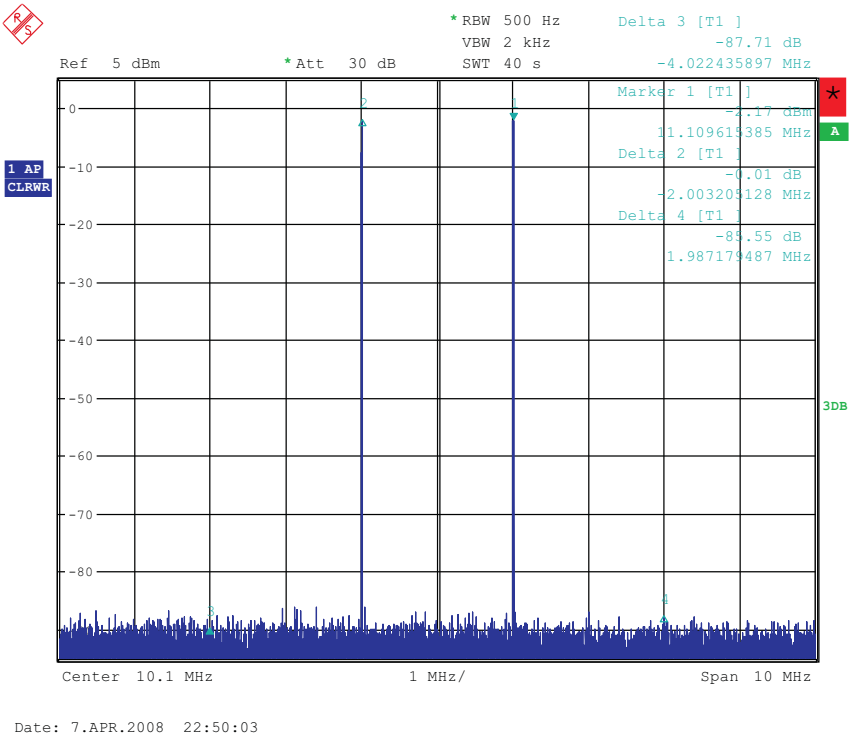


Figure 13. IMD3 Plot for OPA695

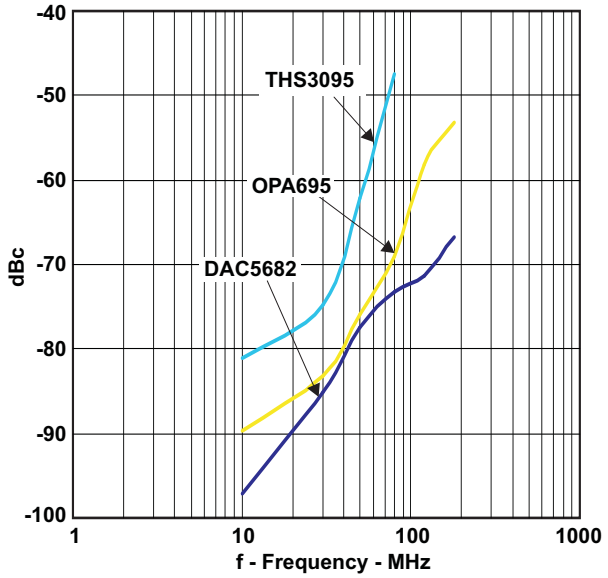


Figure 14. Summary of IMD3 for Passive Transformer, OPA695, and THS3091/5 Output

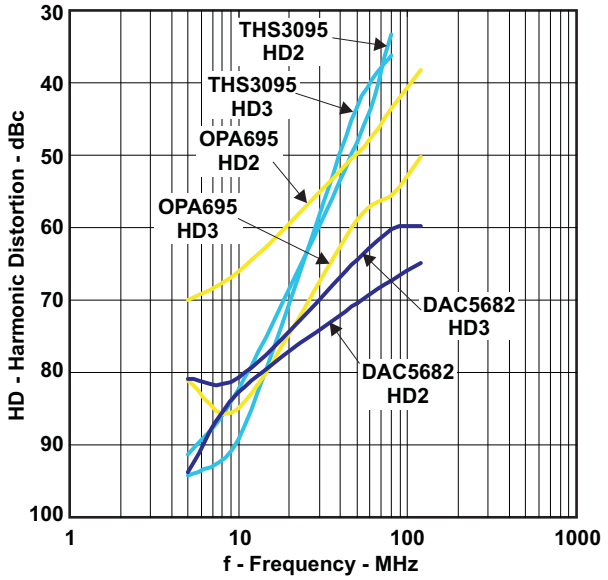


Figure 15. Summary of Harmonic Distortion for Passive Transformer, OPA695, and THS3091/5 Output

8 Initial Power Up and Test

This section outlines the basic power up and test procedure to ensure that the EVM is in an operational state.

8.1 Initial Inspection

Inspect the board to determine which VCXO is on the board. This is useful information when programming the CDCM7005 to lock the DAC clock to the reference. Typically, the board is populated with an 800-MHz VCXO.

8.2 Engage Power Supplies

Plug in the 6-Vdc wall plug.

8.3 Verify Status of the Board

The DAC software will detect if the USB port is active and if it is capable of reading the serial number from the EVM. This determines if the communication between the board and the PC is correct. The HOME menu of the DAC GUI software indicates this status. The VCXO and Reference LEDs (D1, D2) must be lit as well as the power LED (D18).

8.4 Program the CDCM7005

On the DAC5682z EVM GUI, click on "Register Config" which is located on the left side of the GUI. Program the registers as necessary manually or load a saved configuration file. An example file for loading the CDCM7005 called "CDCM7005_4X_Interp.reg7005" can be found on the provided CD. To load this file, click on the "Load Regs" button on the lower center of the GUI. Navigate to the correct location, select this file, then click on "OK". The default mode of GUI has the "CDCM7005 Operation" set to "Buffer Mode". Click on this button and change the setting to "PLL Mode". Next, change the "VCXO Freq (MHz)" default value of "983.04 to "800" by either clicking on the down arrow of this button or entering "800" manually. Hit enter and the new settings will be sent to the CDCM7005. Note that the CDCM7005 LOCK LED (D3) is now lit as it achieves lock between the VCXO and 10-MHz reference. This LED does not illuminate when using external VCXO.

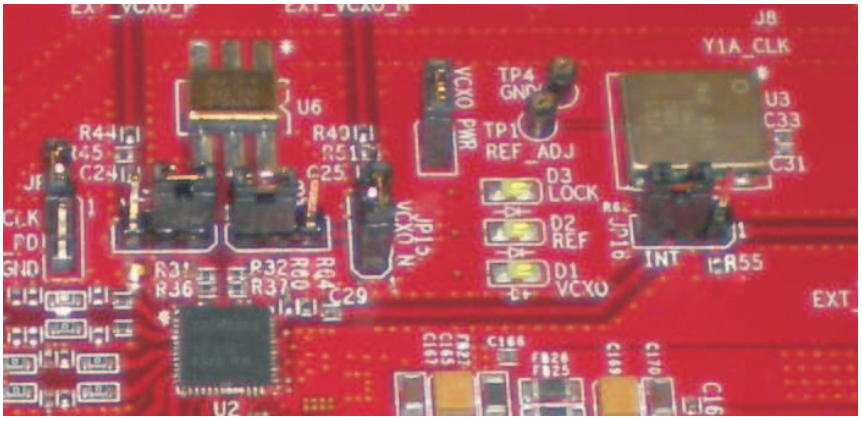


Figure 16. CDCM7005, 800M VCXO, 10M Ref, Locked Condition LEDs

8.5 Program the DAC5682Z

On the DAC5682z EVM GUI, click on "DAC5682 Diagram" which is located on the left side of the GUI. Program the DAC5682z registers as necessary manually or load a saved configuration file. An example file for loading the DAC5682z called "DLL_4X_Interp.reg5682" can be found on the provided CD. To load this file, click on the "Load Regs" button on the right center side of the GUI. Navigate to the correct location, select this file, then click on "OK". The registers will be loaded and the GUI should now look as shown in Figure 17. If the DLL Lock light is red, make sure the pattern generator is providing a proper DCLK to the TSW3070EVM.

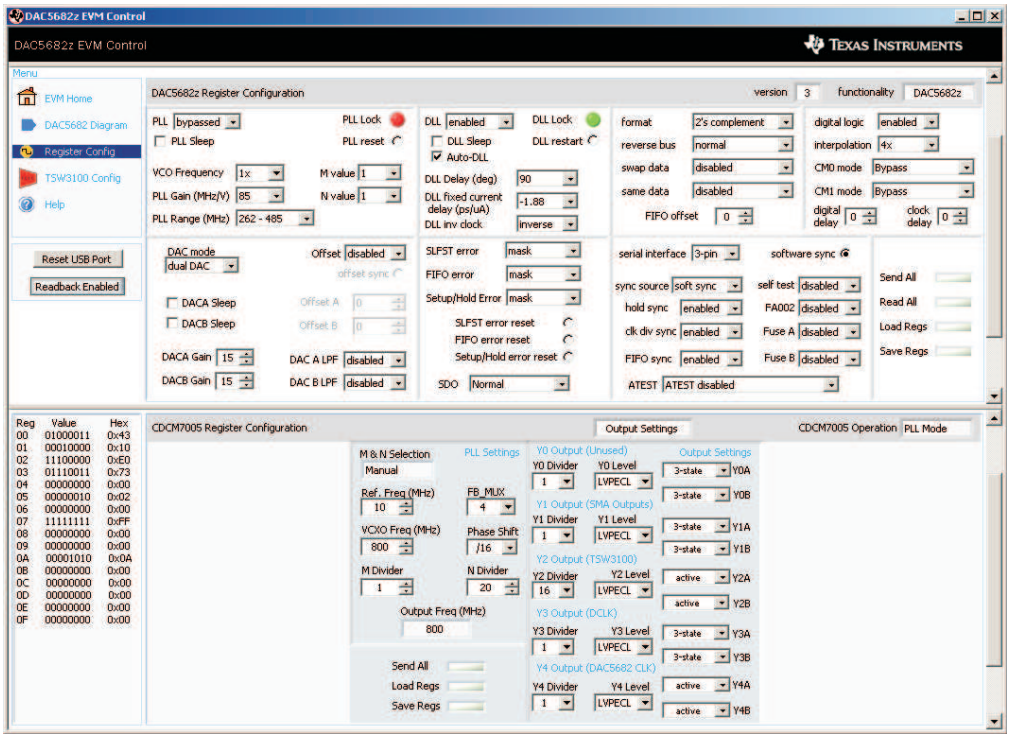


Figure 17. DAC5682 and CDCM7005 Example Register Settings

8.6 Program TSW3100

Use the TSW3100 GUI to generate and load a test pattern, either a tone, multi-tones, or modulated waveforms. This input is required to provide the DCLK to the DAC5682z.

9 Optional Configurations

9.1 External VCXO

It is possible to configure the TSW3070EVM to use an external VCXO for application flexibility. J13 and J14 can be used in position 2-3 to select an external VCXO or clock signal.

9.2 Transformer Passive Output

The board is by default set up to output signals through the OPA695 and THS3091/5. These devices can be individually bypassed to a transformer output, if needed. To bypass the OPA695, move R6 to R109, and R15 to R134. To bypass the THS3091/5, move R20 to R135, and R27 to R136.

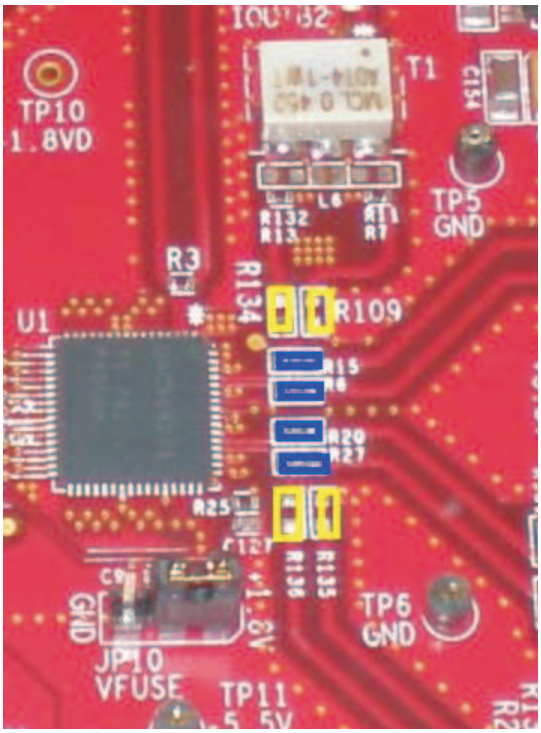


Figure 18. DAC5682Z Resistor Jumper Configuration

The blue denotes the default configuration (operational amplifier output), whereas the yellow denotes the transformer output option.

Table 6. Optional Output Signal Path.

	R109	**R134**	**R15**	**R6**
Bypass OPA695	Install	Install	Remove	Remove
Use OPA695 (default)	Remove	Remove	Install	Install
	R135	**R136**	**R20**	**R27**
Bypass THS3091/5	Install	Install	Remove	Remove
Use THS3095 (default)	Remove	Remove	Install	Install

9.3 Higher Amplifier Voltage Supplies

When changing the amplifier power supplies from the onboard ±5 V to some external supply, it is important to ensure that the voltages to the OPA695 do not exceed ±6.5 V as this could damage the device. When the situation merits, remove the ferrite beads that connect the OPA695 to the ±VAMP supplies (FB10, FB11).

To connect external supplies, the ±VAMP amplifier net must be disconnected from the onboard ±5V net. This involves removing ferrite beads FB7 and FB13. The external supply can then be connected to TP3 and TP9. Keep in mind that the maximum supply voltages for the OPA695 (±6.5V) and the THS3095 (33V between +Vs and –Vs).

	FB7	**FB13**	**FB11**	**FB10**
Internal Supply, Connect VAMP to +/-5V (default)	Install	Install		
Connect OPA695 to VAMP (default)			Install	Install
External Supply, disconnect VAMP from+/-5V	Remove	Remove		
Disconnect OPA695 from VAMP			Remove	Remove

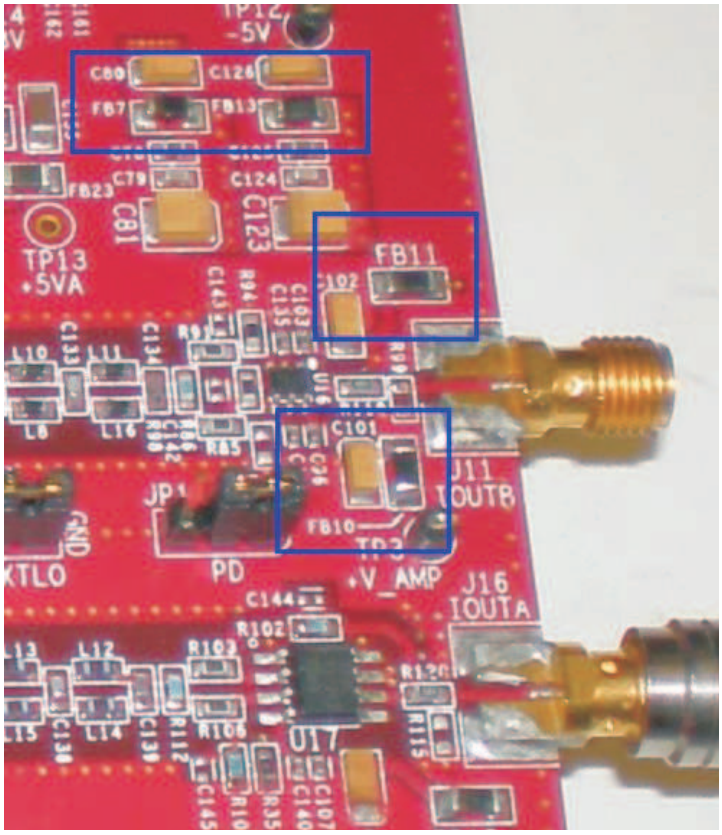


Figure 19. Position of Ferrite Beads for Power Options

9.4 Baseband Filter

The TSW3070EVM has been designed to allow a fifth-order differential LC filter. The filter for the OPA695 is a fifth-order, low-pass filter with a corner at 200 MHz. This filter was designed with a 25-Ω source and termination impedance to account for the DAC load and the operational amplifier input. The THS3091/5 filter is a fifth-order, low-pass filter with a corner at 100 MHz. This filter was designed with a 50-Ω impedance in mind. These filters can only be modified by bearing in mind the design of the DAC termination and operational amplifier configuration. Both outputs of the amplifiers are intended to drive 50-Ω test equipment.

10 Schematic, Bill of Materials and Printed-Circuit Board Layout

The TSW3070EVM schematic, bill of materials, and board CAD design files can be found on the provided compact disc.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -15 V to +15 V and the output voltage range of -15 V to +15 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
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